REMARKS

Claims 6-25 and 36-43 have been cancelled. Claims 1-5, 26-35 and 61-67 are pending. Claims 1-5, 26-35 and 61-67 stand rejected as obvious in view of Chau, Kamath, and Schindler in various combinations. A phone interview discussing the combination of the Chau and Kamath references was conducted on March 23rd. Applicant requests reconsideration of pending claims 1-5, 26-35 and 61-67.

Referring first to claim 1, the claim recites exposing a silicon-comprising surface to activated nitrogen to form a peak nitrogen concentration within the silicon-comprising surface of at least 15% (atom percent). During the interview of March 23rd it was agreed that the above cited references, when viewed as a whole, do not teach or suggest exposing a silicon-comprising surface to activated nitrogen to form a silicon-comprising surface having a peak nitrogen concentration of at least 15%.

Referring first to Chau, a plasma nitridation of a substrate with a power of between 500-2000 watts is described but there is no mention of a peak nitrogen concentration of greater than 5%. In this respect, Kamath is consistent with Chau in that Kamath clearly describes at column 3, lines 15-25 that:

> prior art attempts to increase the nitrogen content have involved forming the gate insulator of a thin amount of silicon dioxide and then annealing the thin silicon dioxide gate insulator in a nitriding ambient such as nitrogen oxide or ammonia. However, **this approach is limited by the thermodynamic limit of the post oxidation annealing process, and typically results in no more than an increase of 2-5 atomic percent nitrogen in the relatively thin silicon dioxide gate insulator**. Increasing the nitrogen content in this limited amount is only of marginal assistance, and obtains only a slight reduction in leakage current. **Moreover, the annealing process also adversely affects the relatively thick silicon dioxide gate insulator of the analog current transistors. The nitrogen atoms introduced by the annealing process introduce charge instability and flicker noise influences which aversely affect the performance and stability of the analog transistors**.

Kamath goes on to recite at Col. 4, lines 1-25 that:

typical silicon nitride based semiconductor fabrication processes involve chemical vapor deposition (CVD) of silane and ammonia on the silicon substrate, or an ammonia reaction with the silicon substrate. **Exposing an already formed silicon dioxide layer to silane or ammonia can create undesirable electrical properties from the nitrogen and hydrogen nitriding the silicon dioxide**.

Further, Kamath describes processes and apparatus that provide both thin silicon nitride based gate insulators and re-oxidized silicon nitride gate insulators (column 4, lines 30-40). The re-oxidized silicon nitride gates preferably contain approximately 20 atomic percent nitrogen to reduce quantum tunneling of carriers (column 5, lines 45-50).

Beginning at column 9 Kamath describes the formation of these silicon nitride and re-oxidized silicon nitride materials. At lines 16-32 Kamath recites that **silicon nitride (64) is deposited by CVD over the entire semiconductor structure, and that the silicon nitride does not nucleate on layer 62 of silicon dioxide**.

Kamath then goes on to recite, at lines 49-65, the formation of re-oxidized silicon nitride by oxidizing silicon nitride layer 64. Kamath recites that **this re-oxidized silicon nitride layer has a nitrogen concentration of more than 20%**.

Kamath cannot be construed to teach nitridation of a silicon-comprising surface to achieve a nitrogen concentration greater than 15%. Consistent with Chau, Kamath recites that only a nitrogen concentration between 2-5% can be achieved by nitridation. Kamath describes no methods for achieving a nitrogen concentration greater than 15% by nitridation. While a concentration of 20% nitrogen is recited by Kamath, it is the concentration of an oxidized silicon nitride layer formed by CVD, not the nitridation of a silicon-comprising surface to achieve a nitrogen concentration greater than 15% as recited in claim 1.

Viewed as a whole, the cited references do not teach or suggest nitridation of a silicon-comprising surface to achieve a nitrogen concentration of 15% within the silicon-comprising surface. Claim 1 is therefore allowable for at least the reason that the cited references, either alone or in combination, do not teach or suggest all of its limitations.

Claims 2-5 depend from claim 1 and are therefore allowable for at least the reasons discussed above regarding claim 1.

Referring next to claim 26, the claim recites, in pertinent part, forming a dielectric material that includes exposing silicon-comprising material to activated nitrogen to form a peak nitrogen concentration within the exposed silicon-comprising material of at least about 15 atom percent. As stated above, the cited references do not teach or suggest this claim limitation and claim 26 is therefore allowable. Applicant requests allowance of claim 26 in the Examiner's next action.

Claims 27-35 all depend from claim 26 and are therefore allowable for at least the reasons discussed above regarding claim 26.

Lastly, Claim 61 recites, in pertinent part, providing a substrate having a surface and incorporating at least 15% nitrogen into the surface by exposing the surface to activated nitrogen. As stated above, the cited references do not teach or suggest this claim limitation and claim 6 is therefore allowable. Applicant requests allowance of claim 61 in the Examiner's next action.

Claims 62-67 depend from claim 61 and are allowable for at least the reason cited above regarding claim 61.

Claims 1-5, 26-35, and 61-67 are believed to be in immediate condition for allowance. Therefore, action to that end is earnestly solicited.

Further, there remains a PTO Form-1449 properly submitted by Applicant which the undersigned has yet to receive an initialed copy from the Examiner. Specifically, on December 18, 2001, Applicant submitted a Supplemental Information Disclosure Statement. A duplicate copy of that Supplemental Information Disclosure Statement and the accompanying PTO Form-1449 is enclosed herewith. It is respectfully requested that the Examiner initial the enclosed Form-1449 and provide the undersigned with a copy of the initialed PTO Form-1449.

Respectfully submitted,

Dated: 4/16/04

By: _____
Robert C. Hyta
Reg. No. 46,791

-END OF DOCUMENT-

Inventor: Zhongze Wang

Title: Methods of Forming Transistor Devices

Assignee: Micron Technology, Inc.

Serial No.: 09/881,407

Filed: June 13, 2001

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

PURSUANT TO 37 C.F.R. §§ 1.56, 1.97 AND 1.98

In compliance with 37 C.F.R. §§ 1.56, 1.97 and 1.98, the Examiner's attention is directed to the reference listed on the attached Form PTO-1449 and a copy of which is attached. No admission is made regarding whether the submitted reference is prior art.

Citation of this reference is respectfully requested.

Respectfully submitted,

Date: 12/14/01

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Form PTO-1449

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

LIST OF ART CITED BY APPLICANT

(Use several sheets if necessary)

ATTY. DOCKET NO.	SERIAL NO.
MI22-1670	09/881,407
APPLICANT	
Zhongze Wang	
FILING DATE	GROUP
June 13, 2001	2811

U.S. PATENT DOCUMENTS

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	6,153,538	11/28/00	An			
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